

OBJECTION TO FIGURES

The Examiner noted that reference numeral 420 is discussed in the specification but is not contained in the drawings.

Applicants respectfully submit that the labeling of reference numeral 420 is now included in FIG. 4, and a replacement FIG. 4 is hereby provided.

REMARKS

In the Office Action, claims 1-24 were rejected. Reconsideration and allowance of all pending claims are requested.

Objection to Drawings

In the Office Action, the drawings were objected to as they did not include a certain reference sign. A replacement sheet correcting the error pointed out by the Examiner is respectfully submitted.

Objection to Specification

The Examiner indicated that the title was considered non-descriptive. Applicants respectfully submit that the title has been now changed to "Static Induction Transistor", which is believed to more clearly indicate the nature of the claimed invention.

Rejections Under 35 U.S.C. §102

The Office Action summarizes claims 1 and 2 as rejected under 35 U.S.C. §102(b) as being anticipated over U.S. Patent 4,799,090, Jun-ichi Nishizawa (hereinafter "Nishizawa"). All of the claims are believed to be patentable for the reasons summarized below.

Claim 1 and Claims Depending Therefrom

Claim 1 recites a transistor switch for a system operating at high frequencies. The transistor switch comprises a graded channel region between a source region and a drain region, the graded channel region configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region; wherein the graded channel comprises at least two doping levels. The transistor switch further includes a gate region extending along a side wall of the graded channel. The gate region is directly in contact with a gate contact. *See*, FIG. 1.

Nishizawa fails to disclose a transistor switch having graded channel region configured for providing a low resistance to mobile negative charge carriers and a gate region extending along a side wall of a the graded channel, the gate region being in direct contact with a gate contact.

Applicants respectfully submit that Nishizawa fails to disclose a graded channel that is configured for providing a low resistance to mobile negative charge carriers. Instead, Nishizawa discloses a transistor that has source region doped with a first conductivity type and the drain region and channel region with the opposite conductivity type. *See*, Nishizawa, FIG. 2, column 3 and lines 19 to 56. Clearly, with such doping patterns, the transistor switch disclosed by Nishizawa provides a path for both *negative carriers and positive carriers*, that is, electrons and holes respectively. Nishizawa fails to disclose a unipolar transistor switch that includes a graded channel for providing a low resistance path to mobile negative charge carriers.

In addition, Nishizawa fails to disclose the gate region extending along the side wall of the graded channel and in direct contact with the gate contact. The gate electrode of the transistor, as disclosed by Nishizawa, controls the n⁺ type region 12 and the n type region 13 which jointly constitute a current path via an insulation film. *See*, Nishizawa, FIG. 2, column 3 and lines 23 to 26. Clearly, the gate electrode is *not in direct contact* with the gate region. Instead, the gate electrode is in contact with the insulation film. *See*, Nishizawa, FIG. 2, FIG. 4, FIG. 5, FIG. 7, FIG. 8 and FIG. 10. Nishizawa fails to disclose a gate region directly in contact with a gate contact.

Because Nishizawa fails to disclose a transistor switch including a graded channel that is configured for providing a low resistance to mobile negative charge carriers and a gate region extending along a side wall of a the graded channel, the gate region being in direct contact with a gate contact, the reference cannot anticipate claim 1. Accordingly, Applicants respectfully submit that independent claim 1 and claims depending therefrom are allowable and respectfully request the Examiner to reconsider the rejection of the claims.

Rejections Under 35 U.S.C. §103

The Office Action further summarizes claims 1, 2, 4-24 as rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Application 2003/0178672, Hatekayama et al. (hereinafter "Hatekayama") in view of U.S. Patent 5,945,701, Siergie et al. (hereinafter "Siergiej").

Independent claims 1 and 16 and Claims Depending Therefrom

Claim 1 recites a transistor switch for a system operating at high frequencies. Claim 16 recites a static induction transistor for a system operating at high frequencies. The transistors recited in claims 1 and 16 include a graded channel region between a source region and a drain region, the graded channel region configured for providing a low resistance to mobile negative charge carriers moving from the source region to the drain region. The graded channel comprises at least two doping levels. The transistor switch further includes a gate region extending along a side wall of the graded channel. The gate region is directly in contact with a gate contact. *See*, FIG. 1.

Applicants respectfully submit that Hatekayama fails to teach or suggest a gate region extending along the side wall of the graded channel and in direct contact with the gate contact as recited in claims 1 and 16. The high breakdown voltage semiconductor device, as disclosed by Hatekayama, includes a gate contact layer that is disposed within a gate region. The gate contact layer has a doping that is different from the gate region. The gate contact layer is in contact with the sidewall insulating film and the gate electrode. *See*, FIG. 1, and paragraphs 68 and 69. In addition, Hatekayama fails to disclose the recited graded channel.

Siergiej fails to obviate the deficiencies in the teachings of Hatekayama. Specifically, Siergiej fails to disclose a gate region extending along the wall of the graded channel. Further, Siergiej fails to disclose a gate electrode directly in contact with the gate region and in direct contact with the gate contact. The gate region, as disclosed by

Siergiej, is not formed within the graded channel but instead is formed outside the channel region. *See*, FIG. 12.

Consequently, the combination of Hatekayama and Siergiej simply cannot render obvious all the recitations of claims 1 and 16.

In view of the following deficiencies in the teachings of the cited art, the Examiner has failed to establish a *prima facie* case of obviousness of claim 1 and claim 16. These claims, and the claims depending therefrom are therefore believed to be clearly patentable over the cited combination. Their reconsideration and allowance are respectfully requested.

Conclusion

In view of the remarks and amendments set forth above, Applicants respectfully request allowance of the pending claims. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: 10/24/2005

Pg
Patrick S. Yoder
Reg. No. 37,479
FLETCHER YODER
P.O. Box 692289
Houston, TX 77269-2289
(281) 970-4545